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Surge suppressors for DC semiconductor switching devices

The recearch including the switching surges at semiconducting switches of commutation apparatus during the time of switching DC circuit. The target of this recearch is to develop a method for calculating the parameters of a switching surge wich consists of series of parallel-connected varistors for using in semiconductor commutation devices. On the basis of recearching the transient processes that can to be in such surge restrictors of voltage in semiconductor switches at DC circuits. mathematical calculation expressions have been proposed for calculating the main parameters of the overvoltage regulator. In the issue, an engineering method allows the calculating the parameters of varistor surge regulators alsow for hybrid and contactless semiconductor apparatus of the DC circuits, and allows to choos lower level of surge admissible for this class of semiconducting devices. The results of the work make it easier high accuracy at a little time in choosing full controlled semiconductor switches with regard to the current and voltage in the design process of modern switching semiconductor apparatus that work in the DC circuits. That helps to solve the basic tasks of apparatus engeneerig. The voltage regulator that is proposed for DC semiconductor switching apparatus allows to limit effectively of switching surges in the power semiconductor devices to below several times by rated voltage level.

Keywords: *switching surge, voltage regulator, varistor, semiconductor apparatus, semiconductor device.*

Introduction. In the end of 20th centure a new stage began in the designing of power electronics. It associated with the development of powerful full controlled semiconductor devices (SDs), in particular a double-gate turn-off (D-GTO) thyristor, a GCT-thyristor (gate communicated turn-off thyristor) and a high-speed power insulated gate bipolar transistor (IGBT-transistor). The high level electronic technology facilitates to organize a growing number of production of those devices in the type of compact integrated module structures as such as IGCTs (GCT-based thyristors) and IGBTs (BTIZ-based thyristors). Theese devices are characterized by high reliability and affordable price. The combination of semiconductor devices and control circuits for them in a single design with different degrees of integration has created excellent conditions to implement various laws of controlling of high level electric energy streams [1, 2].

The mentioned above devices have given a powerful incentive for further development of the hybrid and contactless switching power semiconductor devices (SDs) for the direct current (DC). This apparatus consist in their main circle new fully controlled semiconductor transformers (STs) as switches. The advanced devices have such operational qualities as high switching durability (up to several million cycles), an extremely high speed of performance (only several microseconds), absence of highly expensive and unreliable systems of forced switching, improved functional features, and convenience of combinability with microprocessor devices, which make them really competitive on the world market despite their high cost [3, 4].

These refined DC semiconductor apparatus (SA), contactless [5, 6] and hybrid [7, 8], have switching surges continuously due to the energy stored in the network inductance and the load inductanceduring of commutation. But due to the fact that the circuits at switched off at a significant load during a very short time, the stored energy will be much higher, and dampening it will be more difficult than in earlier developed devices with the capacitive switching of the semiconductor switch. There were the switching capacitor combines its main function with the role of a voltage regulator [9].

In this case, it is rational to research the methods of limiting switch surges in these semiconductor devices and to make relevant calculations. The recearch may be interesting for the developers who professionals working in the electromechanical engineering.

Analysis of recent research and problem statement. In the DC semiconductor apparatus, damping of the switching surge caused by stored energy in the inductance of the electrical network and in the load at the moment of switch-off can be made by the following ways:

– by applying switching condensers [10];
– by using the same condensers wich are shunted with linear resistors [10];
– by applying energy-intensive varistors [11, 12].

In all these methods for diffusion the energy accumulated in the inductive load, it is traditional to use a reverse diode or a reverse thyristor (in the case of a reverse system) which switch simultaneously with the load [13]. Transient electromagnetic processes in semiconductor apparatus have been treated in detail in sufficient [11]. Moreover, it should be noted that due to high energy accumulated in the inductive load at the switching moment, other methods are don't quite fit because it is impossible to use them them (usually the energy accumulated in the inductive load is too higher than the energy accumulated in the electrical network inductance) [14]. Thereby authors shall analyse the above mentioned methods, provided that it is necessary to dampen only the energy accumulated in the network inductance.

The use of capacitors to limit switching surges by transferring the energy accumulated in the circuit inductance into potential energy of the charged capacitors is a classic method implement in DC SA with compulsory capacitive switching of the primary semiconductor switch of the SA made on the basis of thyristors [10]. For obtaining an acceptable level of surge, it is necessary to make use of bulky, expensive impulse capacitors, with a limited temperature working range (it especially electrolytic pulse capacitors). This method can be valid when SA already have capacitive compulsory switching; but in modern SA, which are constructed using fully controlled STs, the implementation of this method is not be expedient [15].

The use of defensive capacitors with linear resistors that are enabled by a special scheme in parallel to the capacitors has allowed significant reduction of their size. Wherein, in addition to the problems connected with deficiencies of the special type of capacitors, there have appeared problems with involving the need to create the schemes for switching linear resistors. They would allow their switching on and off in due time [10]. In that reason this method is also impractical to use for reducing switching surges in modern SA.

Voltage regulators on the basis of the two mentioned above principles are analysed in detail in [10] . The research considers the methods of their calculation subject to constraining switching surges to a level acceptable for SA of the direct current.

In this time, due to the developing of energy-intensive varistors that allow to diffuse the energy of over the hundred kJ and that have suitable size and cost, sufficiently favourable conditions have been designed for their use in modern switching SA for the deffusing of stored energy in the circuit inductance at switching off the device [11, 16].

The mentioned above critical analysis of the different methods of damping switching surges in the power DC switching devices describes that while using DC SA in which STs are fully controlled it is advisable to limit the sharp increase of voltage to the level acceptable for this class of devices, less than 2.5 nominal voltage value U_{nom} [17] by diffusing the energy accumulated in the inductive load by means of the voltage regulator (VR) VR1 on the basis of the feedback diode turned on parallel to the load, and the energy accumulated in the network inductance should be diffused by using VR2 which based on powerful varistors connected to the input circuit of the apparatus.

As are no methods used for calculating varistor VRs integrated into the DC SA using fully controlled power semiconductor devices, there is a need for a detailed researching of the electromagnetic transient processes that take part in the limiters of those devices in time of switching the load. According that, it is necessary to propose a method of calculating the parameters of varistor VRs that reduce switching sharp increase of voltage to the acceptable level for this class of devices.

The purpose and tasks of the study. The target of this study is to develop a method of calculating the parameters of voltage regulators wich consists the the energy-intensive varistors at a given switching surge level in DC SA of the with full-controlled STs.

That is why, it is necessary to determine the following problems:

– to treat transients that occur in the voltage regulators for DC SA at the load switching,

– to solve the analytical expressions to calculate the basic parameters of VRs and to formulate them as the basis of an engineering method of calculation, and

– to propose the examples of calculating the parameters of VRs and switching surges for the most common types of DC SA.

Materials and methods of research. A calculating scheme of circuit of switching voltage regulator is shown in Figure 1.

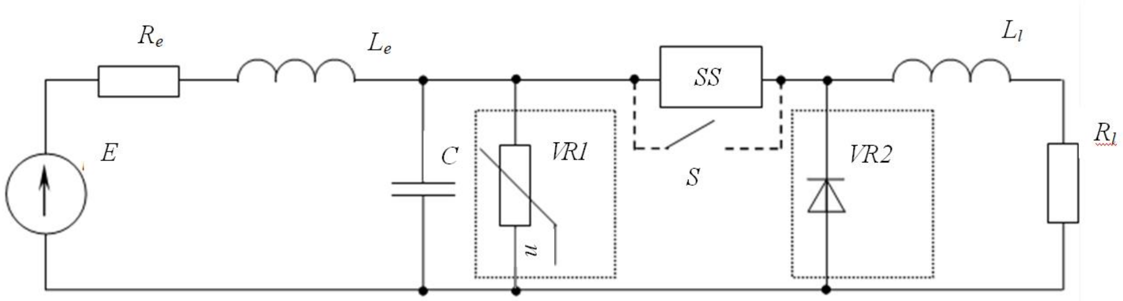

Fig. 1. **An equivalent circuit of switching voltage regulators (SS is a semiconductor switch on fully controlled devices, S is a mechanical switch available only in hybrid apparatus, L_l and R_l are load inductance and active load resistance, whereas L_e and R_e are equivalent inductance and resistance in the circuit)**

The parameters R_e and L_e are calculated in the short circuit mode in the apparatus circuit

$$R_e = \frac{U_{nom}\cdot 1.1}{I_{sc\max}}, \text{ and } L_{sc} = L_e = \tau R_e, \qquad (1)$$

where $U_{ном}$ - the nominal value voltage in the network,
I_{scmax} - the maximum acceptable short circuit current, and
τ - the constant of time of the short circuit current (τ=0.01 s) [17].

In this scheme the capacitor C is the parallel connected to the VR1. That capacitor limits the speed of increase of the switching surge in STs of semiconductor apparatus at the break of the current. The value of capacitor`s capacitance is determined by the following expression

$$C = \frac{I_{SI}}{\left(\frac{du_T}{dt}\right)_{crit}}, \qquad (2)$$

where I_{SI} - the maximum acceptable switched current of the apparatus. (As example, a contactor and a modern high speed circuit breaker this value is usually, $I_{SI}=4\cdot I_{nom.o}$) [4];
$I_{nom.o}$ - a nominal operating current, which is $I_{nom.o}=0.6\cdot I_{nom}$ usually;
$\left(\frac{du_T}{dt}\right)_{crit}$ - a maximum acceptable speed of increase of the current in power semiconductor devices (PSDs).

The parameters of the varistors used in the VR1 have to comply with the math inequalities [4]:

$$\begin{cases} W_{c.\max} < W_{c.adm} \\ I_{c.\max} < I_{c.adm} \\ t_c < t_{adm} \\ U_{cl} \geq \frac{U_{nom}}{0.85}\cdot 1.1 \end{cases}, \tag{3}$$

where t_c - the current duration in the varistor;
$I_{c.adm}$ and t_{adm} - the acceptable amplitude and lasting of the current impulse in the varistor. Its energy W_c does not exceed the acceptable value of energy $W_{c.adm}$;
$W_{c.max}$ - the maximum value of energy diffused in the varistor;
$I_{c.max}$ - the maximum value of current in the varistor;
U_{c1} - a classified voltage of varistor.

For real parameters of the switching circuit of a DC SA, the values of I_c and W_c can be much higher than the acceptable $I_{c.adm}$ and $W_{c.adm}$. As example, for a contactor for I_{nom}=630 A, the maximum switched current I_{sc} in the circuit in the mode of occasional switchings is equal to $4\cdot I_{nom.r}$. Therefore, at $I_{nom.o}=0.6\cdot I_{nom}$, L_e=0.5 mHmH, the accumulated energy of inductance in the electric network is $\frac{L_e I_{SI}^2}{2}=571$ J, while in varistors CH2-2, $W_{c.adm}\leq 150$ J, and in BC2-2 $W_{c.adm.}=350$ J [3].

Therefore, to increase the admissible energy for the VR1, the authors suggest series of parallel connection of a varistors, which is on Figure 2.

This VR consists of n parallel branches. Each of them is containing m serial linked varistors RU1-RUm and one ballast resistor R_b to equalize the currents in the parallel branches.

Computation of the maximum energy make in one varistor of the VR in Fig. 2, a is done for the limiting case of lopsided distribution of current in the parallel branches. It conforms to determining the minimum values of the parameters in an each n-th branch and the maximum values are determined in the other ones.

If current in the n-th branch will be the maximum, the currents in the other branches will be minimal. Clearly that the energy diffused in one varistor proportionally to the squared value of current will be maximal for the varistor that is connected in the n-th branch where is the maximum current.

The calculation of priniple electric scheme of replacing the switching circuit of the VR1 (Fig. 2, a), which has a given distribution of the current, at the stage of limiting the surge looks like in Fig. 2, b (excluding the capacitor current C of the VR1, which has too small a capacity to have any actual effect on the current distribution in the VR1), where L_e is equivalent inductance in the switching circuit ($L_e=L_{sc}$; $R_e\approx 0$); $R_{emax}=m\cdot R_{dmax}+R_{bmax}$ and $U_{emax}=m\cdot U_{cmax}$ are equivalent maximum resistance and voltage in an (n-1)-th branch with the minimum currents i_{cmin}; $R_{emin}=m\cdot R_{dmin}+R_{bmin}$ and $U_{emin}=m\cdot U_{cmin}$ are equivalent minimal resistance and voltage in stabilizing the n-th branch with the maximum currents i_{cmax}; R_{dmax}, R_{dmin} are the max and min dynamic resistances of the varistors; U_{cmax}, U_{cmin} are the max and min voltages in stabilizing the varistors; R_{bmax}, R_{bmin} are the maximum and minimum resistances of the ballast resistor; S1 is the switch simulating the operation of the VR1 (it switches off the branches with the currents i_{cmin} at the declining voltage in the VR1 u_{vr} below U_{emax}).

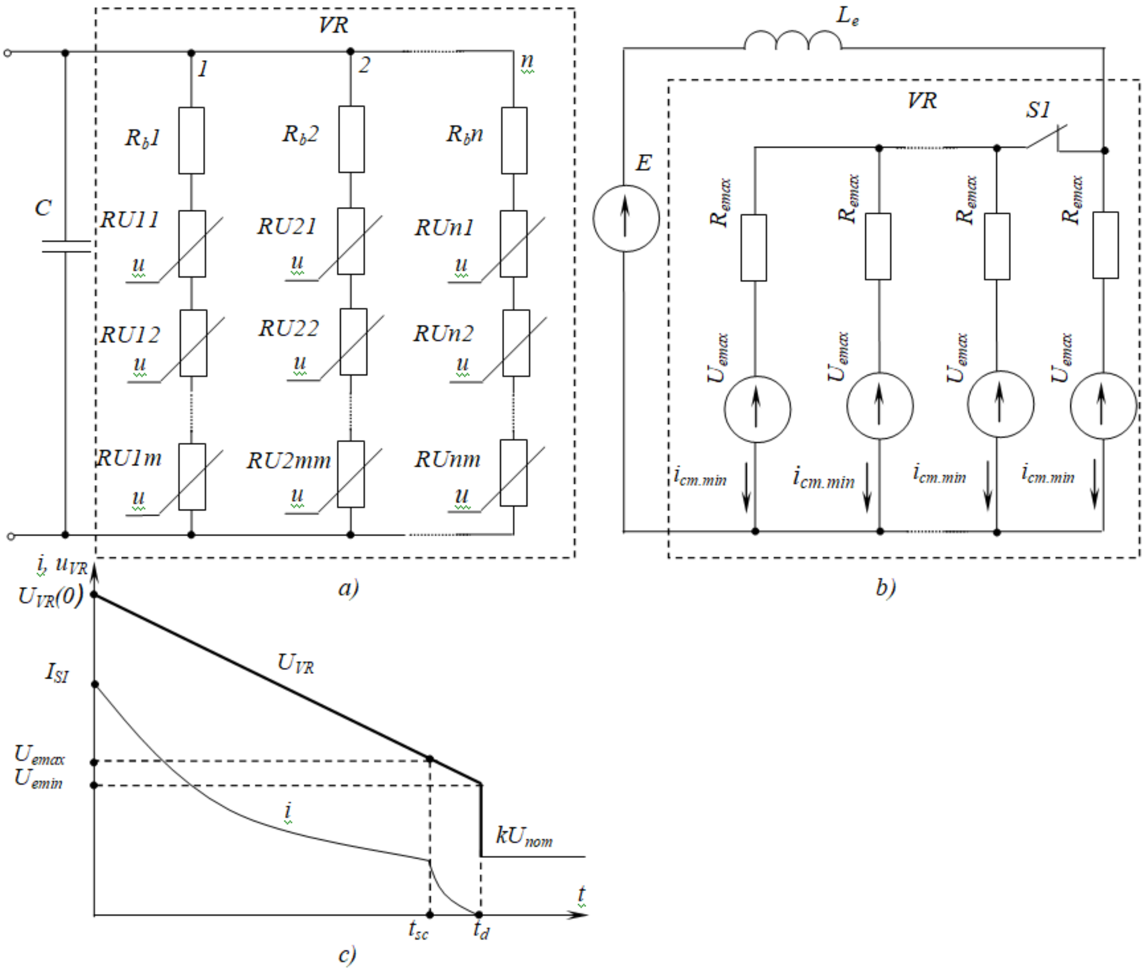

Fig. 2. **The surge suppressor: *a* is a priniple electric scheme of combination of parallel and serial connection of varistors, *b* is a calculation electric scheme of an equivalent switching circuit in the VR, and *c* is the dependency graph of the VR operation**

It is necessary to rise the voltage u_{vr} to the value of U_{emin} for the flowing the current in the VR. Besides the switch S1 can be locked to allow to flow the current in all the *n* branches if the math inequality is like that

$$I_{SI} > (U_{e\max} - U_{e\min}) / R_{e\min}. \tag{4}$$

The practice of using varistors CH2-2 for diffusion big energy in them shows that it is recommendable to choose the varistor`s value U_c as its I-V curve at the current of $I_{1.0}$=1 A. And its dynamic resistance is determined by the expression [4]:

$$R_d = \frac{U_{v100} - U_c}{I_{100}},$$

where U_{v100} - the varistor`s voltage at I_{100}=100 A.

The voltage in the varistor U_v is determined by $U_v=U_c=I_c \cdot R_d$.

Analytical expressions to obtain the basic parameters of the VR and their implementation into the engineering calculation method. To satisfaction the inequality (3), the process in the circuit (Fig. 2, a, $0 \le t \le t_{sc}$) with the locked switch S1 must be in the time interval of $0 \le t \le t_{sc}$ (Fig. 2, c). This is described by the following equations [18]

$$\begin{cases} E = L_e \dfrac{di}{dt} + u_{vr} \\ u_{vr} = U_{e\min} + i_{c.\max} R_{e\min} = U_{e\max} + i_{c.\min} R_{e\max} \\ i = i_{c.\max} + (n-1) i_{c.\min} \end{cases}, \qquad (5)$$

where u_{vr} - the value of voltage on the voltage regulator;
$E = k \cdot U_{ном}$ is the maximum admissible electromotive force (EMF) of the network (k=1.1).

The calculation of the parameters of the protection circuit is shown below.

The solution is subject to the initial condition of $i(0) = I_{SI}$:

$$i_{\tilde{n}\min} = \rho i_{\tilde{n}\max} - I_{imb},$$

$$i = [1 + \rho(n-1)] i_{\tilde{n}\max} - (n-1) I_{imb},$$

$$i_{\tilde{n}\max} = A e^{-t/\tau_{sc}} - I_*,$$

where $\rho = R_{emin}/R_{emax}$;
$I_{imb} = (U_{emax} - U_{emin})/R_{emax}$ - an imbalance current;
$I_* = (U_{emin} - E)/R_{emin}$;
$U_{emin} > E$
$A = I_* + [I_{SI} + I_{imb} \cdot (n-1)] / [1 + \rho \cdot (n-1)]$;
$\tau_{sc} = [(1 + \rho \cdot (n-1)) \cdot L_e] / R_{emin}$.

The amplitude value of the max current in the varistor is

$$I_{\tilde{n}\max} = i_{\tilde{n}\max}(0) = [I_{SI} + (n-1) I_{imb}] / [1 + \rho(n-1)]. \qquad (6)$$

The amplitude value of the limited VR voltage at the device input is

$$U_{v\max} = u_{vr}(0) = R_{e\min} I_{\tilde{n}\max} + Ue_{\min} \le 2.5 U_{nom}. \qquad (7)$$

The duration of the locked state of the switch S can be found by solving the equation $u_{vr} = U_{emax}$

$$t_{sc} = \tau_{sc} \ln \frac{\rho A}{I_{imb} + \rho I_*}. \qquad (8)$$

Also the switch S1 is unlocked and the current i declines to zero at the time interval $0 \le t \le t_{sc}$ (Fig. 2, c). Meantime, the process in the equivalent circuit can be described by the equations [18]

$$E = L_e \frac{di}{dt} + u_{vr}, \; u_{vr} = R_{e\min} i + U_{e\min}.$$

The solution is subject to the elementary condition of $i(0) = I_{imb}/\rho$:

$$i = -I_* + Be^{-t/\tau_{r.s.}},$$

where $B=I_*+I_{imb}/\rho$, $\tau_{r.s.}=L_e/R_{emin}$.

The time of the unlocked mode of the switch S1 can be determined by the equation where i=0

$$t_{r.s.} = \tau_{r.s.} \ln\left(1 + \frac{I_{imb}}{\rho I_*}\right). \qquad (9)$$

The current flow through the VR during the time:

$$t_d = t_{sc} + t_{r.s.}. \qquad (10)$$

The maximum energy $W_{\tilde{n}\max}$ diffused in one varistor in the n-th branch with the current of i_{cmax} is

$$W_{c.\max} = \int_0^{t_{sc}} i_{c.\max}\left(U_{c.\min} + R_{d.\min} i_{c.\max}\right)dt + \int_0^{t_{r.s.}} i\left(U_{c.\min} + R_{e.\min} i\right)dt,$$

or

$$\begin{aligned} W_{c.\max} = &\int_0^{t_{sc}} (Ae^{-t/\tau_{sc}} - I_*)(U_{c.\min} + R_{d.\min}(Ae^{-t/\tau_{sc}} - I_*))dt + \\ &+ \int_0^{t_{r.s.}} (-I_* + Be^{-t/\tau_{r.s.}})(U_{c.\min} + R_{e.\min}(-I_* + Be^{-t/\tau_{r.s.}}))dt \end{aligned}. \qquad (11)$$

The maximum energy $W_{b.max}$ diffused in the ballast resistance in the n-th branch is:

$$W_{b.\max} = \int_0^{t_{sc}} (Ae^{-t/\tau_{sc}} - I_*)^2 R_{b.\min} dt + \int_0^{t_{r.s.}} (-I_* + Be^{-t/\tau_{r.s.}})^2 R_{b.\min} dt. \qquad (12)$$

The minimal energy $W_{\tilde{n}.\min}$ diffused in the varistor in the (n-1)-th branch with the current of $i_{\tilde{n}.\min}$ is:

$$W_{c.\min} = \int_0^{t_{sc}} \left[(Ae^{-t/\tau_{sc}} - I_*)\cdot\rho - I_{imb}\right]\cdot\left[U_{c.\max} + R_{d.\max}\cdot(Ae^{-t/\tau_{sc}} - I_*)\right]dt. \qquad (13)$$

The following engineering method of calculation was suggested on the basis of the obtained expressions in this work.

1. It is initially necessary to select from the VR varistors the type whose main parameters correspond to restriction (3) and then to apply expression (2) to determine the value of the capacitance that shunts the VR.

2. The parameters are defined to calculate the VR operation, provided that the variation in the parameters $U_{\tilde{n}}$, R_d and R_b is with the range of ±5%, and $R_b \approx R_d$.

3. Formula (7) helps to determine $I_{\tilde{n}.\max} \le I_{\tilde{n}.adm.}$ (for the varistor CH2-2 $I_{\tilde{n}.adm} \le 120\,\grave{A}, W_{\tilde{n}.adm} \le 150\,J$).

4. Expression (6) on the basis of the known $I_{\tilde{n}.\max}$ and I_{SI} helps to find out the number of the parallel-connected varistors *n*; the *n* is rounded up to the next whole number. The values of $I_{\tilde{n}.\max}$ and $U_{v.\max}$ are specified.

5. Expressions (8)-(10) defind the time of the current flow through the varistor t_d.

6. Expression (11) determines the maximum value of energy diffuseed in the varistor.

7. If one of the varistor parameters does not meet the accepted confines, the calculation must to be repeated until all varistor settings satisfy the (3) and (7).

The results of calculations on a varistor VR are below. The switching surges determined by the proposed method for the case of using the VR in hybrid DC contactors (for 220 V), which consists common power switching SA.

Calculations were made in Mathcad on the basis of such data: $I_{nom.r}$=0.6·I_{nom}, I_{SI}=4·$I_{nom.r}$ (the maximum current switched by the apparatus in the mode of rare switching), and I_{scmax}=10 mA. In this case, the basic voltage regulating element of the VR is the varistor CH2-2 (330 V).

Table 1 contains the basic parameters for this type of the VR.

Table 1. **The calculation parameters of the voltage regulator**

The nominal contractor current I_{nom}, A	The number of the parallel varistors enable, items	The maximum current of the varistor I_{cmax}, A	The duration of the current flow through the varistor t_d, ms	The maximum switching surge U_{vmax}/U_{nom}	The energy in the varistor		C, μF	R_b, Ω
					U_{cmin}, J	U_{cmax}, J		
100	3	103.60	0.32	2.22	3.71	6.94	1.0	0.68
160	5	105.32	0.50	2.23	6.33	11.56	1.6	
250	7	117.21	0.75	2.30	11.38	19.43	2.2	
400	12	113.37	1.20	2.07	17.90	30.97	3.0	
630	18	118.81	1.85	2.31	29.90	50.34	3.9	

The analysis of the calculation parameters in Table 1 illustrated that the use of inexpensive and compact varistors CH2-2 in creating a VR can limit the level of switching surges to below 2.5·U_{nom} , the using hybrid DC contactors to switch currents equal to 4·$I_{nom.r}$. In this case, even in the loaded contactor (with the effect of the stored circuit energy on the VR) when I_{nom}=630 A, the max energy diffused in the loaded varistor is three times less than the acceptable level, and the mass of the components of the VR is less than 0.1 kg and price is about 10 USD [4].

For example, in the previously developed hybrid contactor KP81-39 (I_{nom}=630 A), the resistive-capacitive VR has 14 parallel capacitors, type K75-17 (1000 V, 50 μF, and the mass of 1.25 kg) [1]. Accordingly, the mass of the VR is at least 17.5 kg, which is bigger than the considered varistor VR. It should be added that the level of restricting voltage surges by this VR amounts to 4.5·U_{nom}, which means that it exceeds the acceptable level for the existing switching devices.

Of course, a varistor VR may be based not only on varistors CH2-2. Other types of varistors and companies can be used if they comply with the requirements. For example, the varistor types SKP6.5.110SA and BYZ50A22.50K39 produced by Semicron. They are designed for U_{c1}=6.5-110 V, they should be enabled in the VR as in a parallel series connection, and the varistor, operating in the most adverse working conditions, must match to the restrictions (3).

Analysis of the research results on switching surges in power DC SA. The main result of the study is that it has developed an engineering method of calculating the parameters of varistor voltage regulators to contactless and hybrid DC SA and given for this devices acceptable surge levels. Also to be noted that the results of this research, as well as studies of the thermal mode of power semiconductor devices in SA [19], facilitate high accuracy at a short time in choosing full-controlled STs with regard to the current and voltage when designing modern switching DC SA. This facilitates to solve the basic tasks of design stages.

But the worry findings in the study are researching only low-voltage SA (up to 1000 V), so it is difficult to extrapolate them onto SA for higher voltage. They have been made possible with the development of high-voltage STs based on silicon carbide [8]. It is expedient to continue research on this issue.

The practical recommendations following from the results of the study and the proposed calculation methods are being used by the developing company ENAS, Kharkiv, Ukraine, to modernize DC hybrid contactors of series KP81. This study refers to the stage of developing design documentation.

Conclusion.

1. The proposed VR with a series of parallel-connected varistors is a highly straight device that effectively limits switching surges in the circuits of power DC SA to below 2.5 U_{nom}. It significantly surpasses such parameters as the dimensions, weight and cost of resistive-capacitive surge limiters previously used in semiconductor commutation apparatus. Moreover, it can reduce the class level of fully controlled PSDs that are used in switches of semiconductor devices for the voltage of 220 V from class 10 down to 6.
2. The proposed engineering method has been developed to compute the VR parameters of varistors in treated voltage regulator. In contrast to the previously researched cases, the present research has considered calculation for only the worst case of distributing varistors in voltage regulator with various deviations of their parameters. This facilitatates to creating VRs on the basis of quite simple calculations to provide a suitable level of switching surges in DC SA in different operation modes, which is quite useful.
3. The calculation method has been proposed in the study can be further used in calculating surges in full-controlled PSDs that apply in an impulse mode as part of power electronic devices.

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Обмежувачі перенапруги для напівпровідникових комутаційних апаратах постійного струму

В роботі показано, що під час перемикання електричних кіл постійного струму на напівпровідникових ключах напівпровідникових апаратів виникають комутаційні перенапруги. Метою цього дослідження є розробка методики розрахунку параметрів обмежувача перенапруг на основі послідовно-паралельного з'єднанння варисторів, що використовується в напівпровідникових комутаційних апаратах. На основі дослідження перехідних процесів, які відбуваються в таких обмежувачах перенапруги напруги в напівпровідникових пристроях при комутації кіл постійного струму, були віднадені аналітичні вирази для розрахунку основних параметрів регулятора напруги. У результаті була розроблена інженерна методика для розрахунку параметрів обмежувачів перенапруги в гібридних і безконтактних напівпровідникових комутаційних апаратах постійного струму. Такі обмежувачі підтримують перенапруги на заданому рівні, який допустимий для пристроїв такого класу. Методика, яка запропонована в роботі за результатами дослідження, забезпечує високу точність та швидкість розрахунку при розробці сучасних перемикаючих напівпровідникових пристроїв, які працюють з у колах постійного струму. Запропонований регулятор напруги для комутаційного напівпровідникового апарату постійного струму ефективно обмежує перенапруги комутації в напівпровідникових пристроях живлення нижче 2,5 від номінальної напруги.

***Ключові слова**: обмежувач перенапруги, комутаційна перенапруга, напівпровідниковий комутаційний апарат, напівпровідниковий прилад, варистор*